

# Samuel A. Kirk

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Fremont CA 94536

## Test Program Development Engineer

Hardware Test Programming / Diagnostic Software & Firmware Development

<http://www.samkirk.com>

### CAREER SUMMARY

- 20+ years in Silicon Valley engineering diagnostic software & firmware, power-on self-test firmware and online and off-line/stand-alone diagnostic software for mixed-signal hardware testing
- Users include hardware design engineers, lab, manufacturing and field technicians

### PROJECTS

- Refined existing, emulator-based DSP code in C for a laser communication controller including on-board dual TMS320C DSPs, SDRAM, Flash and DUART as test targets. Screened all prototype electronics hardware (both analog and digital) prior to integration into electro-optics laser communication system, developing a 100+ page manual test procedure. There were *no* escapees! Wrote trouble-shooting code for failed boards as needed for the hardware technician and engineers. Developed test automation for the wavefront sensor using Scilab and AutoHotKey. Performed Mil-Spec 810F Testing for the complete electronics laser communications subsystem including not only the controller and the wave-front sensor but also the hi-voltage amplifier, the tip-tilt mirror driver and the membrane mirror oscillator/reference laser boards.
- Ported UltraSPARC T1 CPU POST to the telco-oriented ATCA chassis from a business enterprise platform. Similarly ported UltraSPARC VF CPU POST to a telco-rugged, NEBS-qualified chassis. Also ported online diagnostics for both service processors, MPC885-based running Linux
- Closed over 20 bugs on ethernet loopback test program spanning all of Sun's platforms as Mr. "netlbtst" of SunVTS. Ported detailed register-level simulation tests for dual-ported, 10 Gbps, UltraSPARC-embedded Network Interface Unit (NIU) to standalone, online IODiag program for silicon verification.
- Developed custom test equipment and software for performance verification of source synchronous, receive-only channels for an ATE instrument in DDR and Hyper Transport testing up to 3.2 Gb/sec.
- Developed an on-line diagnostic for an Edge Measurement Calibration Subsystem (ECMS) in an ATE chip tester having an accuracy within 1.5 pico-seconds a 3-dimensional, linear regression algorithm. Ran early versions of this diagnostic prior to any hardware in the Verilog co-sim environment with Catalyst Image.
- Expanded control software for single-die probing into multi-die probing for 2- & 4-die parallel testing. Debugged the master/slave tester box interface card connected to a hardware emulator for 3 slaves. The master program consisted of 9 files in 6500 lines in Object Pascal. The slave Mac program consisted of 30,000 lines of code in 18 files.

### TECHNICAL SKILLS

C/C++, Image, UML, SPC, Six Sigma, Forth, Tcl/Tk, SystemC, Tiger Catalyst, UNIX, Linux, SLED 10, ClearCase, ClearQuest, MacOS, DOS, Windows, SCSI, PCI, VMEBus, JTAG, Unix I/O Drivers, UltraSPARC T1 & VF, TMS320C, MC680X0, MC5600X, MC68332, MPC8260, MPC883, i808X, MicroChip PIC, ARM, MIPS, 6 Sigma

### PROFESSIONAL EXPERIENCE

**Sr. Diagnostic Software Engineer**, AOptix Technologies, Campbell, CA.....2008 ~ 2009  
**Diagnostic Software Engineer**, Sun Microsystems, Santa Clara, CA.....2006 ~ 2008  
**Test Development Engineer**, Teradyne, San Jose, CA .....2002 ~ 2005  
**Chief Technology Officer**, Pacific Beta Corporation, Fremont CA.....2001 ~ 2002  
**Chief Consulting Engineer**, Samuel A. Kirk Consulting, Fremont CA .....1998 ~ 2000  
**Senior Audio Test Software Engineer**, ESS Technology, Fremont CA .....1994 ~ 1998  
**Senior Diagnostic Software Engineer**, Media Vision, Fremont CA.....1992 ~ 1994

### EDUCATION

**MS, Computer & Systems Sciences**, University of Louisville, Louisville, KY  
**BA, Philosophy & Mathematics**, Ohio State University, Columbus, OH  
**Statistical Process Control (SPC)**, Principles & Applications, Silicon Valley Technical Inst. San Jose, CA

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- Ported an entire suite of analog tests written for a Sentry-based load board into highly readable, manageable routines written for a superset load board. Wrote detailed register-level description of the load board and created hi-level, block diagrams to explain and confirm its hi-level operation. Supported the code in the wafer sort environment as well as the single-slave standalone environment.
- Created 230 macros implemented in 4800 lines of 56001-based assembly code for all of the digital functional testing. Test routines were scripted in a special pseudo language comprising 50 pages of text and implemented in 11,400 lines of the macro-assembly code.
- Debugged using a Tektronix PRISM 3000 logic analyzer with 80 channels attached to the DSP and another 80 attached to the DUT card with two full digital scope channels for debugging in the analog domain.
- Developed and supported manufacturing test software for PC-based audio cards and video capture cards for multi-media PC computing as the sole test development engineer for manufacturing test at the board level in the entire company.
- Made over 20 releases of this test software for audio and 3 releases for video capture hardware. Released test software ranging from 3 days to 2 weeks after availability of functional hardware prototypes and DOS device driver utility software.
- Reduced test cycle time to 60 seconds per board including setup and take down while increasing overall test coverage.
- Completely specified a standardized, PC-based functional test station. Supported off-shore facilities in Taiwan, Singapore and Hong Kong as well as local out-of-house fab facilities through in-house product engineers and manufacturing engineers.
- Developed test firmware for mfg signature analysis of a SPARC-based home-theater system which included an audio subsystem with 16 DSPs and micro-sequencer-based move engine in a SPARC-based, hi-end home theater system.
- Developed fast stream table tests for the audio DSP subsystem as well as a power-up test for the SCSI disk drive. Integrated separate tests into Auto Test firmware for manufacturing burn-in. Created specialized firmware packages for diagnosing "dead" boxes.
- Created test cases in Windows for a Host Signal Processing (HSP) 56K modem prototype. Developed in an extreme programming development environment using a prototype implemented in a large Xilinx FPGA array. Did turn-arounds on an almost daily basis.
- Created Power-On POST firmware for 4 different MC68332-based controllers in a sports/entertainment robot and for the communications network that served them in the field.
- Wrote test routines in the package to check the core of each controller: an instruction set of the CPU, a checksum test of the ROM, address test (and variations) of the static RAM. Also wrote loopback tests for the serial controller present on each board and for specialized peripherals (ADCs and an LCD).
- Designed and developed embedded POST firmware and a standalone/off-line diagnostic software package for an MC68020 CPU in ROLM's 8750 Computerized Branch Exchange (CBX).
- Designed and developed an on-line diagnostic program for remote satellite telephone switch inter-links in a digital, Class 5 telephone switch.
- Led a standalone release of diagnostic software for a multiple processor file server. Wrote the entire software release description for it, performed make files to SQA's standards and tracked all bugs.
- Developed test routines for an 8-minute analog storage cell device in which each cell in this device stored one of 256 voltage levels for 8-to-1 compression ratio. Implemented a device driver in DSP code that explicitly toggled in each serial bit.
- Served as advisor to the DMTF working group on the Common Diagnostics Model (CDM).